What is claimed is:

1. A data processor, comprising:

a central processing unit; and

an address translation unit that receives a virtual addresses output from said central processing unit and outputs a physical address,

wherein said address translation unit includes a first translation lookaside buffer, a second translation lookaside buffer, and a control circuit for selecting one of said first and second translation lookaside buffers and performing address translation in accordance with an area of an address space in said virtual address.

2. A data processor according to claim 1,

wherein each of said first and second translation lookaside buffers has a plurality of entries for holding predetermined physical addresses associated with a predetermined virtual address respectively for performing the address translation,

wherein said central processing unit is capable of accessing a first virtual address space and a second virtual address space included in the virtual address space,

wherein said first translation lookaside buffer translates said virtual address of said first virtual address space to said physical address, and

wherein said second translation lookaside buffer translates said virtual address of said second virtual address space to said physical address.

3. A data processor according to claim 2,

wherein a part of entry means of said plurality of entries in said second translation lookaside buffer is, even when said second translation lookaside buffer detects an address translation miss, disabled from rewriting the physical address stored in the entry, and

wherein the remaining entries of said plurality of entries in said second translation lookaside buffer are enabled to rewrite the physical address stored in the entry at an address translation miss.

4. A data processor according to claim 3,

wherein said part of entry means that is disabled from rewriting said physical address in said second translation lookaside buffer stores a physical address for storing an address translation miss handling routine.

5. A data processor according to claim 4,

wherein it is determined whether or not said plurality of entries in said second translation lookaside buffer should be rewritten at an address translation miss in accordance with said address translation miss handling routine.

6. A data processor according to claim 1,

wherein said control circuit decodes upper bits of the virtual address output from said central processing unit and selects one of said first and second translation lookaside buffers in accordance with a decode result.

7. A data processor according to claim 1,

wherein said address translation unit further includes a selection circuit to which a first output of said first translation lookaside buffer and a second output of the second translation lookaside buffer are input, and which selects one of said first and second outputs in accordance with the control signal of said control circuit and outputs as said physical address.

8. A data processor according to claim 1,

wherein said address translation unit further includes an address chop circuit that fixedly forms said physical address from said virtual address when both of said first and second translation lookaside buffers are disabled.

9. A data processor according to claim 1,

wherein a page size of said first translation lookaside buffer is different from a size of said second translation lookaside buffer at translation from the virtual address to the physical address.

10. A data processor according to claim 2,

wherein the number of said plurality of entries included in said first translation lookaside buffer is adapted so as to be larger than the number of said plurality of entries included in said second translation lookaside buffer, and

wherein a page size when said first translation lookaside buffer translates said virtual address of said first virtual address space to said physical address is adapted so as to be smaller than a page size when said second translation lookaside buffer translates said virtual address of said second virtual address space to said physical address.

11. A data processor according to claim 2,

wherein said address translation unit further includes a third translation lookaside buffer having a plurality of entries for holding a predetermined physical address associated with a predetermined virtual address for performing address translation, and

wherein said plurality of entries of said third translation lookaside buffer is capable of storing both of a copy of a part of the entries of said plurality of entries in said first address buffer and a copy of a part of the entries of said plurality of entries in said second address buffer.

12. A data processor according to claim 11,

wherein said third address buffer is capable of operating selectively in accordance with instruction fetch operation of said central processing unit so as to perform address translation processing in parallel with said first and second translation lookaside buffers.

13. A data processor, comprising:

a central processing unit; and

an address translation unit that receives virtual addresses output from said central processing unit and outputs a physical address,

wherein said address translation unit includes a first translation lookaside buffer for performing address translation of a first virtual address space in said virtual addresses, a second translation lookaside buffer for performing address translation of a second virtual address space in said virtual addresses, and a control circuit for selecting any one of the said first and second translation lookaside buffers in accordance with which of said first and second virtual address spaces said virtual address belongs to and performing address translation.

14. A data processor according to claim 1,

wherein each of said first and second translation lookaside buffers includes a plurality of entries for holding a predetermined physical address, respectively, associated with a predetermined virtual address for performing address translation.

15. A data processor according to claim 1,

wherein said second translation lookaside buffer stores a physical address for storing an address translation miss handling routine of said first translation lookaside buffer, and an entry for storing the physical address is disabled from rewriting.

16. An IP module including information of a microprocessor module, comprising:

data for defining an address translation unit for receiving a virtual address output from a predetermined central processing unit and outputs a physical address,

wherein said address translation unit includes a first translation lookaside buffer, a second translation lookaside buffer, and a control circuit for selecting one of said first and second translation lookaside buffers and for performing address translation in accordance with an area of an address space in said virtual address.

17. An IP module according to claim 16,

wherein each of said first and second translation lookaside buffers has a plurality of entries for holding predetermined physical addresses associated with a predetermined virtual address respectively for performing the address translation,

wherein said central processing unit is capable of accessing a first virtual address space and a second virtual address space included in the virtual address space,

wherein said first translation lookaside buffer translates said virtual address of said first virtual address space to said physical address, and

wherein said second translation lookaside buffer translates said virtual address of said second virtual address space to said physical address.

18. An IP module according to claim 17,

wherein a part of entry means of said plurality of entries in said second translation lookaside buffer is, even when said second translation lookaside buffer detects an address translation miss, disabled from rewriting the physical address stored in the entry, and

the remaining entries of said plurality of entries are enabled to rewrite the physical address stored in the entry at an address translation miss.